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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,800	02/24/2004	Chen-Yu Liu	26019	9751

7590 11/15/2005

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EXAMINER	
QI, ZHI QIANG	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,800	LIU, CHEN-YU	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *4,7-9,14,17,19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,10-13,15,16 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/16/04;*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of restriction in the reply filed on Oct.6, 2005 is acknowledged. The traversal is on the ground(s) that applicant request withdrawal of the restriction requirement. This is not found persuasive because the claims contain different embodiment that constitutes different species as the pixel electrode are zigzag and the common electrodes are not overlap the data line, the pixel electrode are linear and the common electrode are not overlap the data line, and the pixel electrode are zigzag and the common electrodes are overlap the data line that would need further searches.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 4,7-9,14,17,19-20 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected claims, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on Oct.6, 2005.

Claim Objections

3. Claim 10 is objected to because of the following informalities: recitation, ". . .a passivation layer on said space, . . ." in which the "space" does not have any definition in the claim. For examination purpose, it is interpreted as a passivation layer on said plurality of sources, said plurality of drains, and said insulating layer. Appropriate correction is required.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by US 5,886.762 (Lee et al).

Regarding claim 10, Lee discloses (col.7, line 32 – col.9, line 5, Figs.4-5) that a liquid crystal display panel comprising:

- an upper substrate, a lower substrate (1) parallel to the upper substrate, a liquid crystal layer between the two substrates;
- a plurality of common lines (the counter electrode 2B-1 functions as the common line) and a plurality of gate lines (2A) on the substrate (1) and parallel each other;

- an insulating layer (gate insulation film 3) on the substrate (1) and the common line (2B-1) and the gate line (2A);
- a semiconductor layer (4) on the insulating layer (3) and above the gate line (2A);
- a plurality of source (5A-1) and a plurality of drain (5B-1) respectively on two sides of the semiconductor layer (4) above one corresponding gate line (2A);
- a plurality of data lines (5A) on the insulating layer (3) perpendicular to the plurality of gate lines (2A) and electrically connected to one corresponding source (5A-1);
- a passivation layer (protective film 31 functions as the passivation layer) on the plurality of sources (5A-1) and the plurality of drains (5B-1) and the insulating layer (3);
- a plurality of transparent inter-digital pixel electrodes (7) on the passivation layer (31), each of the transparent inter-digital pixel electrode having first fingers (branches 71,72,73,74,75) that extend in the direction parallel to the data lines (5A) and are electrically connected to one corresponding drain (5B-1) through at least one first contact hole (C1);
- a plurality of transparent inter-digital counter electrodes (6) on the passivation layer (31), one side of each of the plurality of transparent inter-digital pixel counter electrodes (6) having second fingers (branches 62,63,664,65) that extend in the direction parallel to the data lines (5A) and are electrically

connected to one corresponding common line (2B-1) through at least one second contact hole (C);

- a pixel region is defined by one of the date lines (5A) and one of the gate lines (2A), at least one first contact hole (C1) and at least one second contact hole (C) are on the same side of the pixel region, and the first fingers and the second fingers are interlaced in the pixel region.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3,5-6,11-13 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,886.762 (Lee et al) in view of US 6,914,645 B2 (Kurahashi et al)

Regarding claims 1 and 11, Lee teaches the invention set forth above. Lee further discloses (col.7, line 32 – col.9, line 5, Figs.4-5) that a liquid crystal display panel comprising a plurality of thin film transistors on the lower substrate (1), and each of the thin film transistor is positioned near a respective intersection portion of the gate lines (2A) and the data lines (5A). Lee does not explicitly disclose a planar insulating layer on the passivation layer (a planar insulating layer among the passivation layer, the pixel

electrode ,and the common electrode), so that the pixel electrodes and the common electrodes are on the planar insulating layer.

Kurahashi discloses (col.7, lines 3-29; Fig.1) that the passivation film (PSV) has a stacked structure, PSV1 and PSV2. Therefore, the PSV2 functions as a planar insulating layer on a passivation layer (PSV1) (a planar insulating layer among the passivation layer PSV1, the pixel electrode PX and the common electrode CT). Kurahashi indicates (co.l.7, lines 14-29) the passivation film (PSV) avoiding direct contact between the thin film transistor (TFT) and the liquid crystal, so as to prevent the characteristic degradation of the thin film transistors. As a general available knowledge, the stacked structure of passivation layer would provide more protection, and using passivation layer (PSV2) as planar insulating layer would improve the surface flatness.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display panel of Lee with the teachings of using two passivation layers and the top passivation layer as a planar insulating layer so that the pixel electrode and the common electrode on the planar insulating layer as taught by Kurahashi, since the skilled in the art would be motivated for more protection and improving the surface flatness.

Regarding claims 2,5,12 and15, Lee discloses (col.3, lines 1-45) that the transparent pixel electrodes and the transparent common electrodes are made of ITO.

Regarding claims 3,6,13 and 16, Lee teaches the invention set forth above except for the first fingers (branches of pixel electrodes) and the second fingers (branches of common electrodes) are zigzag.

Kurahashi discloses (col.8, lines 43-67; Fig.3) that the pixel electrode (PX) and the common electrode (CT) are zigzag, and made of a plurality of bends so that compensating for the tinting of an image depending on viewing angles.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display panel of Lee with the teachings of zigzag pixel electrodes and common electrodes as taught by Kurahashi, since the skilled in the art would be motivated for compensating the viewing angle characteristics.

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Kurahashi as applied to claims 1-3,5-6,10-13 and 15-16 above, and further in view of US 6,184,946 B1 (Ando et al).

Regarding claim 18, Lee and Kurahashi teach the invention set forth above except for a doped amorphous silicon layer having two portions between the insulating layer and the sources and between the insulating layer and the drains respectively.

However, in order to form thin film transistor, forming a doped amorphous silicon layer between the insulating layer and the sources and between the insulating layer and the drains that is conventional.

As an evidence, Ando discloses (col.4, lines 17-29; Fig.1) that a doped amorphous silicon layer (16) as an electric contact layer having two portions between the insulating layer (13) and the sources (18) and between the insulating layer (13) and the drains (17) respectively that is conventional to form a thin film transistor.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display panel of Lee and Kurahashi with

the teachings of forming a doped amorphous silicon layer as taught by Ando, since forming a doped amorphous silicon layer as an electric contact layer is an conventional technique to form a thin film transistor.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Qi
November 9, 2005

ANDREW SCHECHTER
PRIMARY EXAMINER